AMENDMENTS TO THE CLAIMS

Listing of the claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Claims 1-3 (Canceled)

4. (Currently Amended) A semiconductor memory device, ~~with~~ comprising:

a plurality of subblocks, each ~~including a drive circuit and a memory array, the device~~ comprising[[:]] a memory array and a drive circuit driving lines of memory cells therein, the lines including a redundant line for repair;

an address input circuit for receiving an address signal input;

~~a drive circuit for driving the plurality of subblocks in compliance with the address signal;~~

~~a signal line for connecting the address input circuit and the drive circuit;~~

a defective line information store circuit for storing defective line information showing defective lines in [[a]] the plurality of subblocks ~~according to subblocks~~;

a redundant circuit, located proximate to the drive circuit of each of the plurality of subblocks and comprising a volatile storage circuit, for substituting ~~other~~ one of the lines including [[a]] the redundant line of the corresponding subblock for a defective line in ~~each of the plurality of subblocks~~ that subblock according to the state of the volatile storage circuit;

common signal lines for connecting the defective line information store circuit and the redundant circuit corresponding to each subblock and for connecting the address input circuit and the drive circuit of each subblock to deliver the address signal input; and

a supply circuit for ~~supplying~~ transferring the defective line information ~~stored in~~ from the defective line information store circuit to the volatile storage circuit in the redundant circuit corresponding to each subblock via the ~~signal line,~~ common signal lines.

~~wherein the redundant circuit includes a storage circuit for storing the information supplied from the defective line information store circuit, and makes the substitution on the basis of the information stored in the storage circuit.~~

5. (Original) The semiconductor memory device according to claim 4, wherein the defective line information store circuit is shared by a plurality of subblocks.

6. (Original) The semiconductor memory device according to claim 5, wherein the plurality of subblocks which share the defective line information store circuit are located in the direction perpendicular to the line.

7. (Currently Amended) The semiconductor memory device according to claim 5, wherein each of the plurality of subblocks is divided into a plurality of sections, further wherein the redundant circuit performs ~~a redundant process~~ the substitution in each of the plurality of sections.

8. (Previously Presented) The semiconductor memory device according to claim 4, wherein the defective line information store circuit is located proximate to a side of one of the plurality of subblocks parallel to the defective line.

9. (Canceled)

10. (Currently Amended) The semiconductor memory device according to claim [[9]] 4, wherein the drive circuit is located along a side of ~~one of the plurality of subblocks~~ the corresponding memory array, further wherein the ~~signal line is located~~ common signal lines run parallel to the drive circuit.